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PATENT ABSTRACTS OF JAPAN

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(54) **CHARGED-PARTICLE-BEAM TESTING APPARATUS AND
SEMICONDUCTOR-INTEGRATED-CIRCUIT TESTING APPARATUS**

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(57)Abstract:

PURPOSE: To obtain an LSI image in which an abnormal portion can be detected easily.

CONSTITUTION: A trigger signal is generated at the beginning of every test pattern, it is delayed by a set delay amount by a delay means 23, electron-beam pulses are directed to an IC 15 by its delayed output, and their secondary electrons are detected by a detector 16 and taken in by one out of memories 18, 19 as image data. It is repeated at every horizontal scanning operation to increase a delay amount by a definite amount at every trigger. When data of one frame is acquired, an acquisition completion signal is sent to a signal generator 11. Whenever the signal generator 11 receives the acquisition completion signal, it alternately

changes an operating condition such as a power-supply voltage, and it makes the same test. In addition, a condition signal is generated, and the storage of the image data is changed over alternately between the memories 18, 19, and the difference in the data between the memories 18, 19 is displayed.

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CLAIMS

[Claim(s)]

[Claim 1] In the charged-particle line testing device which irradiates a charged-particle line in pulse at a working semiconductor integrated circuit, detects the secondary electron, and obtains the image of potential distribution of the above-mentioned semiconductor integrated circuit A trigger signal is received from the stimulus generator which supplies a performance test signal to the above-mentioned semiconductor integrated circuit. A delay means to give the horizontal to the above-mentioned semiconductor integrated circuit by the charged-particle line or a vertical-scanning location, and the corresponding delay to the trigger signal, and to generate a charged-particle line pulse, The charged-particle line testing device characterized by providing the means which changes the are recording field of the image data obtained from the above-mentioned detection secondary electron whenever it receives the condition signal which shows that the operating condition of a semiconductor integrated circuit was changed from the above-mentioned stimulus generator.

[Claim 2] It consists of a stimulus generator and a charged-particle line testing device. A performance test signal from the above-mentioned stimulus generator Supply the semiconductor integrated circuit in the above-mentioned charged-particle line testing device, and the semiconductor integrated circuit is operated. In the semiconductor integrated circuit testing device which irradiates a charged-particle line to the above-mentioned semiconductor integrated circuit in pulse with the above-mentioned charged-particle line testing device, detects the secondary electron working, and obtains the image of potential distribution of the above-mentioned semiconductor integrated circuit A means to transmit the trigger signal which shows the criteria to the above-mentioned stimulus generator for every repetition of the above-mentioned stimulus to the above-mentioned charged-particle line testing device, If the operating condition of the above-mentioned semiconductor integrated circuit is made to change, it will have a means to transmit the condition signal which shows that to the above-mentioned charged-particle line testing device. A delay means to give the horizontal to the above-mentioned semiconductor integrated circuit by the charged-particle line or a vertical-scanning location, and the corresponding delay to the above-mentioned trigger signal which received to the

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above-mentioned charged-particle line testing device, and to generate a charged-particle line pulse, the above-mentioned condition signal is received -- ** -- the means which changes the are recording field of the image data which was boiled and was obtained from the above-mentioned detection secondary electron -- having -- ***** -- the semiconductor integrated circuit testing device characterized by things.

[Claim 3] The testing device according to claim 1 or 2 characterized by providing a means to display the difference of both the image data accumulated in the above-mentioned image data accumulation field.

[Claim 4] The testing device according to claim 3 characterized by providing the means which indicates a means to memorize the pattern configuration information on the above-mentioned semiconductor integrated circuit, and the above-mentioned pattern configuration information and the above-mentioned difference image data by superposition.

[Claim 5] The above-mentioned delay means is a testing device according to claim 1 to 4 characterized by being a means to make it add and to perform the above-mentioned delay the amount of predetermined delay every to the amount of setting delay for every unit migration of the above-mentioned horizontal or a vertical scanning.

[Claim 6] The testing device according to claim 5 characterized by making random the above-mentioned perpendicular or a horizontal scanning.

[Claim 7] It is the testing device indicated to claim 1 characterized by being a means to have a means to make the scan to the above-mentioned semiconductor integrated circuit perform at random, and for the above-mentioned delay means to read the lag data memorized beforehand according to the horizontal or vertical position in the above-mentioned random scan, and to set the above-mentioned trigger signal as the delayed delay circuit thru/or either of 4.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] It is related with the testing device used for this invention irradiating charged-particle lines, such as an electron beam and an ion beam, at a semiconductor integrated circuit, measuring the amount of the secondary electron to generate, displaying potential distribution of that semiconductor integrated circuit as a shade image, and judging a defect part etc.

[0002]

[Description of the Prior Art] For example, in an electron beam testing device, an electron beam is irradiated at a working semiconductor integrated circuit (it is described as Following IC), the amount of the secondary electron then generated is measured, an electron beam exposure location is shifted for that one by one about the same test pattern, and displaying the shade image according to the amount of a secondary electron is performed. Although the circuit pattern images 1-4 of IC appear as the display image in this case is shown for example, in drawing 7 A, there are few secondary electrons from wiring with which high-level potential is given, and they are displayed black like the pattern images 1 and 2 in a display image. On the other hand, there are many secondary electrons from wiring with which low potential is given, and it is displayed white like the pattern images 3 and 4 in a display image, and the generating secondary electron is the middle of the each secondary electron in a high-level part and a low part, and parts 15 other than wiring are displayed on gray. The image of drawing 6 A is called stroboscope image.

[0003] Since the impression test pattern corresponding to this display image is known, that is, the potential of the forward always of each wiring is known, this display image can be seen and it can judge whether that IC is operating correctly or which part is unusual. Moreover, it is performed that an axis of abscissa forms the image in which the location of a horizontal scanning line and the time-axis of a stimulus are shown as the location horizontal scanning of the electron beam is carried out between the timing points set up from the timing point which the stimulus set up, a horizontal scanning line is shifted one by one, and carries out a vertical scanning for said every timing point of

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both, for example, it is shown in drawing 7 A. In drawing 7 A, stimulus 1a which shows a circuit pattern image to correspondence wiring at drawing 7 B is impressed. the timing point T0 from -- T1 The circuit pattern image 1 shows aging of the potential of the wiring which can be set. by -- T0 [therefore,] from -- part deltaT1 of a low the circuit pattern image 1 -- the first white part L1 It is displayed. ***** -- The following high-level part deltaT2 The next part L2 of the circuit pattern image 1 It is displayed as a part for Kurobe and the following low part is displayed as a following white part L3 in the circuit pattern image 1. Stimuli 2a and 3a are impressed to correspondence wiring, respectively, and the circuit pattern images 2 and 3 are the timing point T0. Or T1 It is an image corresponding to between. Thus, the image which also displayed time amount change of a stimulus is called the LSM image. This can know the condition of a temporal response on one screen.

[0004]

[Problem(s) to be Solved by the Invention] when obtaining the image shown in drawing 6 A, in order to make the SN ratio high, when the same image is repeated and acquired, a charge collects on the insulating protective coat of the front face of IC, and it is shown in 6B and 6C -- as -- the distinction with the circuit pattern image of a high level, and the circuit pattern image of a low -- it cannot do -- becoming -- just -- being alike -- it will become the display of the same gray. Therefore, the thing of a high SN ratio was not able to be obtained.

[0005] Moreover, as shown in drawing 6 A, when taking in the data in the setting pattern of a stimulus, the condition of the change based on impression of the test pattern with the passage of time cannot be known. However, although this can be known by the LSM image, as drawing 7 was described previously, when obtaining an LSM image and it repeats and acquired on the same conditions, the image was able to become not clear and an SN ratio was not able to be raised.

[0006] Furthermore, many images needed to be acquired in IC in which the sequential circuit holding actuation and the logical circuit which does not hold actuation are established in two or more **** to get to know the defect generating timing in the defect's generating stage (location) and stimulus.

[0007]

[Means for Solving the Problem] According to this invention, the trigger signal which received from the stimulus generator is delayed with a delay means, a charged-particle line pulse is generated, but that amount of delay is set up corresponding to the horizontal to IC by the charged-particle line, or a vertical-scanning location. Moreover, whenever it receives the condition signal which shows that the operating condition of IC was changed from the stimulus generator, the are recording field of image data is changed. A change of this operating condition is made whenever it acquires the image data of the specified quantity, for example, the data for one screen.

[0008] The display of image data may superimpose and display the image data of this difference, and the pattern configuration information on IC, when displaying the thing under acquisition actually and displaying the difference of both the image data in two are recording fields. The delay by the delay

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means is made to add the amount of predetermined delay every to the amount of setting delay for every [horizontally or] unit migration of a vertical scanning. Or IC is made to scan at random, the lag data beforehand memorized in the horizontal or the vertical position is read to the random equipment, and it is carried out by setting the lag data as a delay circuit.

[0009]

[Example] The example of this invention is shown in drawing 1 . The stimulus generator 12 is connected to this testing device 11 by the case where an electron beam testing device is used as a charged-particle line testing device 11. In the electron beam testing device 11, an electron beam 14 is generated in the shape of a pulse within the vacuum chamber 13, and IC15 in a chamber 13 irradiates. The secondary electron generated by the exposure is detected by the secondary electron detector 16, and is memorized with the change means 17 as image data by either of the image memories 18 and 19.

[0010] A test pattern signal, a power-source signal, etc. which were generated from the test pattern generating section 21 in a stimulus generator are supplied to IC15 as a stimulus, and IC15 operates based on this. Synchronizing with a repetition of the test pattern signal that is, a trigger signal is supplied to the delay means 23 in the electron beam testing device 11 from the trigger signal generating section 22 at the beginning of each test pattern signal. Furthermore, modification of the operating condition to ICs15, such as supply voltage of operation, supplies the condition signal which shows that from the condition signal generator 24 to the control section 25 of the electron beam testing device 11. Although not shown in drawing, the various test conditions of the electron beam testing device 11 can be set up to a control section 25, and a control section 25 controls each part according to the setup. It is controlled by the control section 25, an electron beam 14 is controlled by these scan means 26 and 27, and the X-scanning means 26 and Y scan means 27 also carry out the part to which IC15 was set a horizontal and a vertical scanning.

[0011] For example, the stimulus shown in drawing 2 A is generated, and it is generated as a trigger signal shows drawing 2 B at the repetition time. it is shown in a control section 25 to a trigger signal at drawing 2 C -- as -- timing point T0 from -- T1 up to, if it is set up as incorporation of data and the incorporated number of data which takes lessons from 1 horizontal scanning line is set up with N individual Unit time amount deltat of $(T1-T0) / (N-1)$ is called for, and the amount of delay of the delay means 23 is $t1 = T0$. It is initialized. the first trigger signal -- the delay means 23 -- $t1 = T0$ only -- it is delayed, and is inputted into a pulse generator 29, the pulse of an electron beam 14 is discharged by the pulse generated from this, and the secondary electron of IC15 is detected. It is $t1 = T0$ as shown in drawing 2 D for every trigger signal below. It receives, the electron beam pulse for which only deltat was delayed mostly one by one is discharged, and incorporation of image data is performed. Moreover, an electron beam 14 is horizontally moved by 1 pixel for every incorporation of this 1 image data. That is, whenever an electron beam 14 is horizontally moved by 1 pixel by the X-scanning means 26, the amount of setting delay in the delay means 23 is added only for deltat .

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[0012] Thus, it is timing T0 -T1 by one horizontal scanning. After the image data which can be set is incorporated, image data is incorporated the whole horizontal scanning similarly and the incorporation of the image data for one screen is completed, the completion signal of acquisition is sent out to the stimulus generator 12. If this acquisition signal is received, the stimulus generator 12 changes IC operating condition, for example, changes supply voltage into 4V from 5V, and generates a condition signal, a stimulus and a trigger signal are generated similarly again, and as drawing 2 was described, the electron beam testing device 11 will discharge the electron beam pulse from which timing shifted one by one for every trigger signal, and will perform incorporation of image data.

[0013] The completion signal of acquisition is generated for every acquisition of the image data for one screen like the following, an operating condition is changed by turns for every reception of the completion signal of acquisition, and it repeats generating a condition signal, a stimulus, and a trigger signal. Moreover, the incorporation of image data is changed to image memories 18 and 19 by turns for every reception of a condition signal. When the supply voltage of IC15 of operation is 5V, it is timing point T0 -T1. The potential change on wiring 1' of a between, 2', and 3' changes with the curves 1a, 2a, and 3a of drawing 3 A, and this considers as normal actuation. On the other hand, when a condition change of the supply voltage is made 4V, it is timing point T0 -T1. The potential change on wiring 1' of a between, 2', and 3' presupposes that it came to be shown in the curves 1a, 2a, and 3a of drawing 3 B. that is, wiring 1' -- the polarity of a potential pattern -- reversed -- wiring 2' -- the same potential pattern -- becoming -- wiring 3b -- the timing point T2 - T3 only -- the polarity was reversed.

[0014] When image data is repeatedly acquired in such a condition and each of that image data is displayed on a display 31, the acquisition image in the all seems well of drawing 3 A comes to be shown in drawing 3 C. That is, the circuit pattern image 1 is displayed on white by the low of curvilinear 1a, and is displayed on black with a high level. Curvilinear 2a does not have relation to a low and a high level, and since this used as gray serves as the same potential curve even if supply voltage of operation changes to 4V, and the potential condition over the location and time amount in wiring 2' does not change irrespective of the change of an operating condition, the circuit pattern image 2 is for the charge over a protection insulator layer to arise, that is, is the same as that of the case where it points out on the trouble of the conventional technique. The circuit pattern image 3 is the timing point T1 - T3. In the corresponding low of the section L23, it becomes white, and since change does not arise in the change of an operating condition about a location and time amount, other parts serve as gray.

[0015] On the other hand, the acquisition image in the abnormal condition of drawing 3 B comes to be shown in drawing 3 R>3D. That is, the circuit pattern image 1 is the section T2 of curvilinear 3a when it became gray at since black was displayed with the high level of curvilinear 1a, white was displayed by the low and the circuit pattern image 2 was changeless like the case of drawing 3 C, and

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change produced the circuit pattern image 3 in the change of operation - T3. In a high level and the corresponding part L23, the parts of black and others serve as gray.

[0016] Thus, if operating state is changed and supply voltage is lowered to 4V in this example from drawing 3 C and D, in wiring 1', it will be understood that always [forward] and having completely become a reverse display and having become abnormalities were understood, and they moreover always differed from always [forward] also regarding the place and with time. However, it also turns out that abnormalities do not arise at all in wiring 2', and they are timing T2 - T3 in the part L23 on wiring 3' at wiring 3'. It is understood that only the section was set to a high level from the low with abnormalities.

[0017] Furthermore, when the image data shown in drawing 3 C is subtracted from the image data shown in drawing 3 D and the image data of the difference is displayed, it comes to be shown in drawing 4 A. That is, as for the parts L04 and L56 from which the low of forward always turned into a high level, the high level of forward always is displayed for the circuit pattern image 1 on black by white, as for the parts L45 and L61 which became at the low. Even if it changes an operating condition, the circuit pattern image 2 used as abnormalities does not appear at all on the screen. Only the part L23 set to a high level from the low about wiring 3' serves as black, and other parts do not appear at all. The display of this drawing 4 A appears more clearly [the thing used as abnormalities] than the display of drawing 3 C and D. Although precision is inferior for a while, since each circuit pattern image also appears to the display of drawing 4 A, drawing 3 C and D understands the location of a defect part, and a time location for the display condition of abnormalities well.

[0018] If the potential of wiring 1' lowers supply voltage of operation to 4V by of operation supply voltage 5V in curvilinear 1a of drawing 4 B, when it takes with a low, the part T23 from which a high level turned into a low like the image L23 in drawing 4 C in said difference image data image will be displayed on white like curvilinear 1a' of drawing 4 B. Furthermore, when T24 is set to a low by the fall of supply voltage like curvilinear 1a" in the first half of the high-level part in curvilinear 1a, only the part T24 of a difference image appears as a white image L24. Furthermore, curvilinear 1a" If T43 is set to a low like in the second half of the high-level part of curvilinear 1a, only a part T43 will serve as the white image L43, and a difference image will appear. Thus, aging of wiring potential can also be known in this invention. In addition, curvilinear 1a" and 1a" Each **** serves as black and a white display by the stroboscope image, respectively.

[0019] By carrying out the electron beam scan of the front face, detecting a secondary electron, or carrying out a repetition electron beam scan, detecting a secondary electron, while it has been in a fixed condition, although a stimulus is impressed, and obtaining a stroboscope image in the condition of not operating IC15, etc. About IC part which acquires the configuration information on the front face of IC15 (image data), that is, corresponds with the display of for example, drawing 3 C It enables it to display the circuit pattern images 1, 2, and 3 of wiring 1', 2', and 3' in two main tracks,

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respectively, as shown in drawing 4 D. The part which should be observed is displayed clearly and it can be easy to read the location on that IC by memorizing this configuration information in memory 32, and superimposing and displaying this configuration information and difference image data (drawing 4 A and correspondence).

[0020] although the exposure timing of an electron beam was made to increase Δt every with horizontal migration of an electron beam in **** (i.e., although image data was acquired so that the horizontal direction on the screen might serve as a time-axis), image data may be acquired so that it may become a time-axis perpendicularly. In this case, on the same horizontal scanning line of an electron beam, it is constant value t_i about the electron beam exposure timing to a trigger signal. It carries out, and on the following horizontal scanning line, only Δt delays electron beam exposure timing and an electron beam is irradiated to the timing of $t_i + \Delta t$ to a trigger signal. In addition, in one horizontal scanning, whenever it acquires 1 image data so that the same point may not be irradiated, only Δt is good to carry out initiation of a horizontal scanning early.

[0021] when making the exposure timing of an electron beam increase Δt every during 1 horizontal scanning, a vertical scanning may be made to perform at random, i.e., the number of a horizontal scanning line is put in order at random, and sequential selection of the horizontal scanning wire gage put in order is made for every horizontal scanning. Moreover, when acquiring image data so that a time-axis may become perpendicular as mentioned above, you may make it irradiate an electron beam in the pixel location which put each horizontal scanning in order at random and chose each pixel location number on the line as the order put in order for it. Like, by performing a vertical scanning at random, these things [carrying out the electron beam exposure of level or the near part continuously] are avoided, and can lessen effect of charge of a protection insulator layer. this technique -- especially -- a location -- it is effective when making resolution high.

[0022] A horizontal and a vertical scanning may be similarly made random. For example, as shown in drawing 5 , data required for making each point on a horizontal scanning deflect an electron beam are memorized by the horizontal deflection register 34, data required for making each point on a vertical scanning deflect an electron beam are memorized by the vertical deflection register 35, and the data in which the electron beam exposure timing (the amount of delay to a trigger signal) to each pixel on 1 horizontal scanning line is shown are memorized by the delay register 36. The number which shows the location of each point of all scan layers is generated from the random generator 36. The horizontal deflection register 34 and the delay register 36 make a high order bit the address by making the lower bit into the address, and the vertical deflection register 35 is read, respectively. The data read from the horizontal deflection register 34 are changed into an analog signal with DA converter 38, and horizontal deflecting system is supplied. The data read from the vertical deflection register 35 are changed into an analog signal with DA converter 39, a vertical deflection machine is supplied, it is set as the delay circuit 41 where the data read from the delay register 36 are delayed in a trigger signal,

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and the output of the delay circuit 41 is supplied to a pulse generator 29.

[0023] In ***, although the image data in two operating conditions is acquired by turns, about the thing of the same operating condition, averaging can be carried out, respectively and an SN ratio can also be raised. Although time amount required to incorporate the image data for one screen is based also on setups, it is not necessary to expect the greatest time amount, to change an operating condition automatically by the stimulus generator 12 side, and to generate the completion signal of acquisition in the electron beam testing-device 11 side. Although the operating condition was changed for every acquisition of the data for one screen, an operating condition may be changed for every predetermined acquisition of the data for a screen, such as every acquisition of the data for a half-screen.

[0024]

[Effect of the Invention] Since the LSM image data for a predetermined screen are changed for operating conditions, such as supply voltage and a test pattern clock frequency, by turns for every acquisition according to this invention as stated above, the place currently observed can be obtained clearly, without being influenced by the insulating protective coat.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The block diagram showing the example of this invention.

[Drawing 2] Drawing showing the stimulus in actuation of drawing 1, a trigger signal, an image data acquisition period, and a related example with electron beam pulse irradiation timing.

[Drawing 3] Drawing in which A and B show the example of a signal on wiring, and C and D are drawings showing the example of a display of correspondence acquisition image data, respectively.

[Drawing 4] Drawing in which A shows the example of a display of difference image data, drawing in which B shows the normal signal and its various abnormality signals on wiring, drawing showing the corresponding display image with each abnormality signal [in / in C / B], and D are drawings showing the example of the display screen of the surface type-like information on IC.

[Drawing 5] The block diagram showing the example of a random scan signal generation means and the corresponding delay means 23.

[Drawing 6] Drawing showing the example of stroboscope image display for explaining the trouble in equipment conventionally.

[Drawing 7] Drawing in which A shows the example of an LSM image display, and B are drawings showing the signal on the correspondence wiring.

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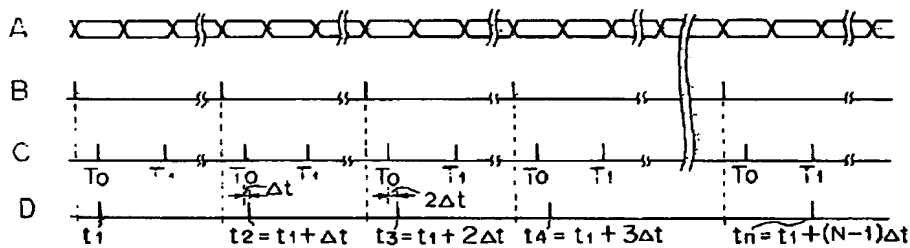
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DRAWINGS

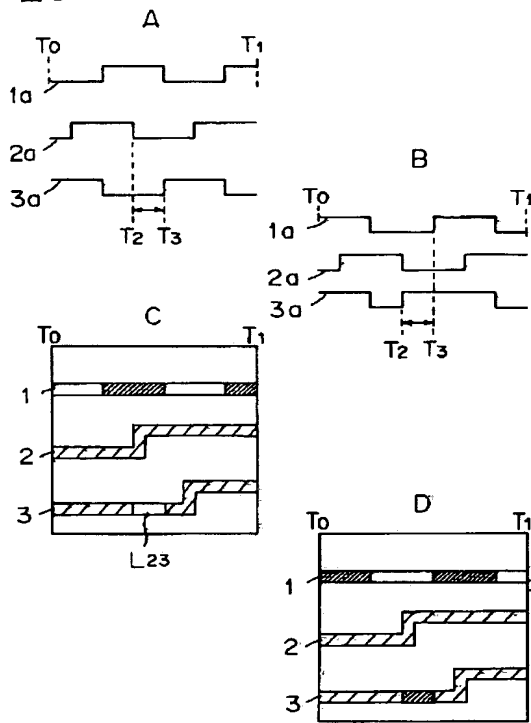
图 2

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[Drawing 3]

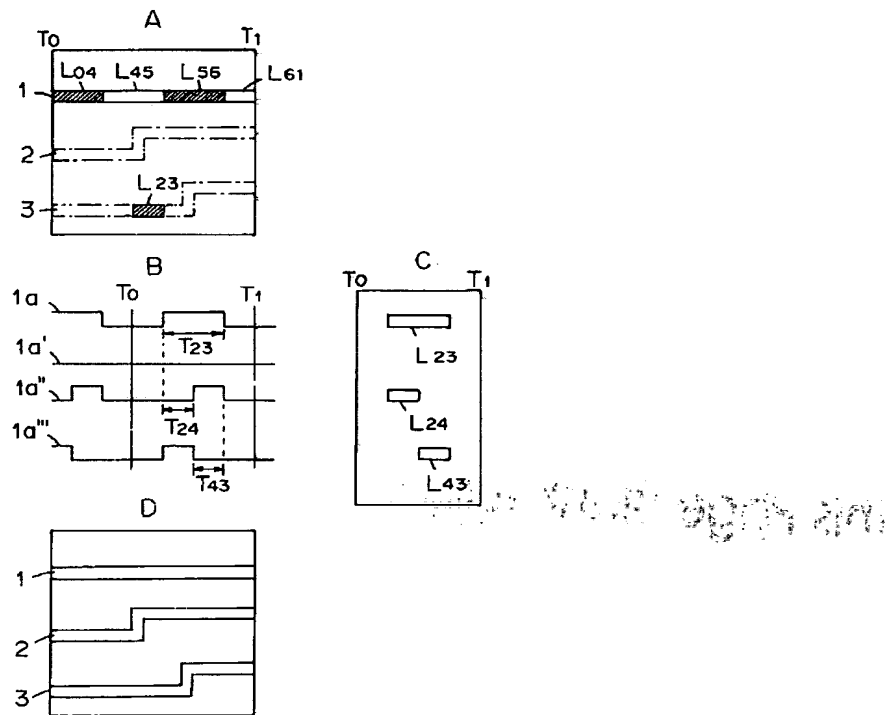
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[Drawing 4]

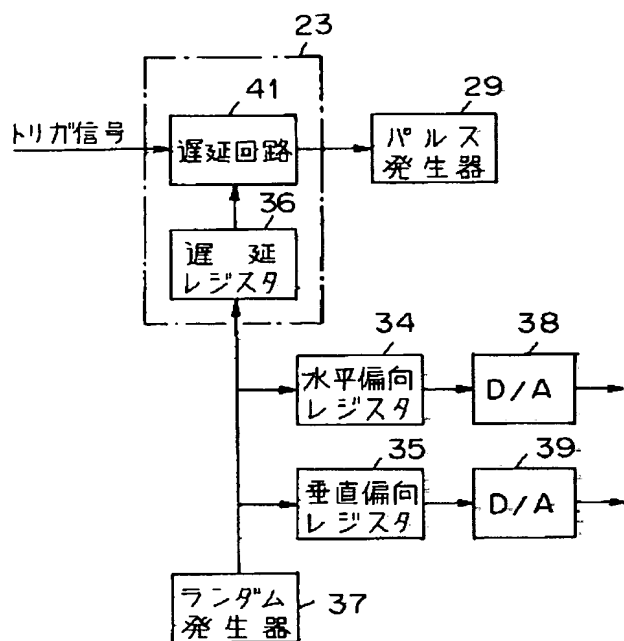
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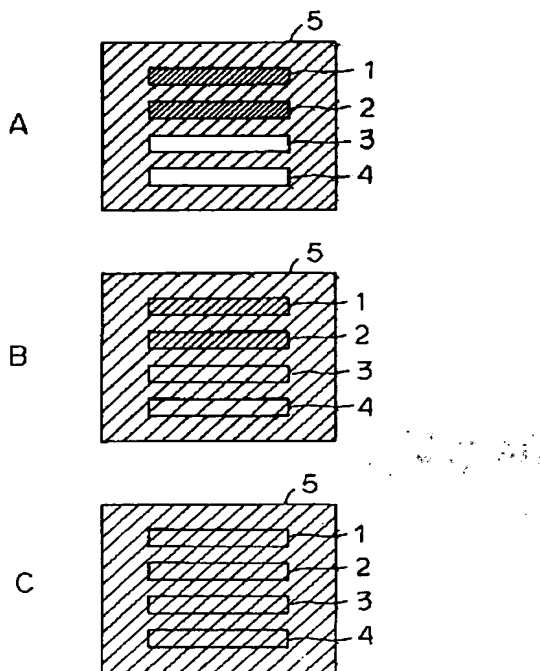
[Drawing 5]

図 5



[Drawing 6]

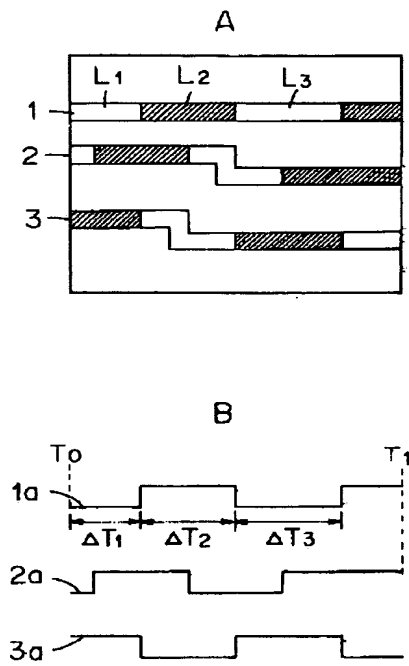
図 6



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[Drawing 7]

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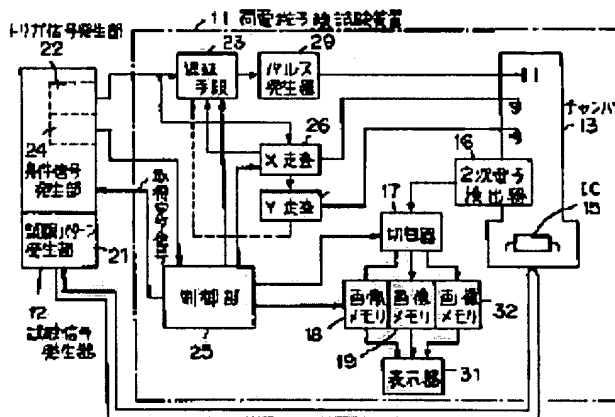
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Applicant: ADVANTEST CORP
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- **International:** G01R31/302; G01N23/225; H01L21/66
- **European:**
Application number: JP19930301618 19931201
Priority number(s): JP19930301618 19931201

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PURPOSE: To obtain an LSI image in which an abnormal portion can be detected easily.

CONSTITUTION: A trigger signal is generated at the beginning of every test pattern, it is delayed by a set delay amount by a delay means 23, electron-beam pulses are directed to an IC 15 by its delayed output, and their secondary electrons are detected by a detector 16 and taken in by one out of memories 18, 19 as image data. It is repeated at every horizontal scanning operation to increase a delay amount by a definite amount at every trigger. When data of one frame is acquired, an acquisition completion signal is sent to a signal generator 11. Whenever the signal generator 11 receives the acquisition completion signal, it alternately changes an operating condition such as a power-supply voltage, and it makes the same test. In addition, a condition signal is generated, and the storage of the image data is changed over alternately between the memories 18, 19, and the difference in the data between the memories 18, 19 is displayed.



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【特許請求の範囲】

【請求項1】 動作中の半導体集積回路に荷電粒子線をパルスの的に照射し、その2次電子を検出して、上記半導体集積回路の電位分布の画像を得る荷電粒子線試験装置において、

上記半導体集積回路へ動作試験信号を供給する試験信号発生器からトリガ信号を受信し、そのトリガ信号に対し、荷電粒子線による上記半導体集積回路に対する水平又は垂直走査位置と対応した遅延を与えて荷電粒子線パルスを発生させる遅延手段と、

上記試験信号発生器から半導体集積回路の動作条件を変更したことを示す条件信号を受信するごとに、上記検出2次電子より得た画像データの蓄積領域を切り替える手段と、

を具備することを特徴とする荷電粒子線試験装置。

【請求項2】 試験信号発生器と荷電粒子線試験装置とよりなり、

上記試験信号発生器から動作試験信号を、上記荷電粒子線試験装置内の半導体集積回路へ供給してその半導体集積回路を動作させ、

その動作中に、上記荷電粒子線試験装置で荷電粒子線をパルスのに上記半導体集積回路へ照射し、その2次電子を検出して上記半導体集積回路の電位分布の画像を得る半導体集積回路試験装置において、

上記試験信号発生器に上記試験信号のくり返しごとに、その基準を示すトリガ信号を、上記荷電粒子線試験装置へ送信する手段と、

上記半導体集積回路の動作条件を変更させると、そのことを示す条件信号を上記荷電粒子線試験装置へ送信する手段とを備え、

上記荷電粒子線試験装置に受信した上記トリガ信号に対し、荷電粒子線による上記半導体集積回路に対する水平又は垂直走査位置と対応した遅延を与えて荷電粒子線パルスを発生させる遅延手段と、

上記条件信号を受信するごとに、上記検出2次電子より得た画像データの蓄積領域を切り替える手段とを備え、

上記条件信号を受信するごとに、上記検出2次電子より得た画像データの差を表示する手段を具備することを特徴とする請求項1又は2記載の試験装置。

【請求項4】 上記半導体集積回路のパターン形状情報を記憶する手段と、上記パターン形状情報と上記差画像データとを重畳表示する手段を具備することを特徴とする請求項3記載の試験装置。

【請求項5】 上記遅延手段は、上記水平又は垂直走査の単位移動ごとに、設定遅延量に対し所定遅延量ずつ加算させて、上記遅延を行う手段であることを特徴とする請求項1乃至4のいずれかに記載の試験装置。

【請求項6】 上記垂直又は水平走査がランダムにされることを特徴とする請求項5記載の試験装置。

【請求項7】 上記半導体集積回路に対する走査をランダムに行わせる手段を備え、上記遅延手段は上記ランダム走査における水平又は垂直位置に応じて、予め記憶された遅延データを読み出して、上記トリガ信号を遅延する遅延回路に設定する手段であることを特徴とする請求項1乃至4のいずれかに記載した試験装置。

【発明の詳細な説明】

【0001】

【産業上の利用分野】 この発明は電子ビームやイオンビーム等の荷電粒子線を半導体集積回路に照射し、発生する2次電子の量を測定し、その半導体集積回路の電位分布を濃淡画像として表示して不良部分を判定すること等に用いられる試験装置に関する。

【0002】

【従来の技術】 例えば、電子ビーム試験装置において動作中の半導体集積回路（以下ICと記す）に電子ビームを照射し、そのとき発生する2次電子の量を測定し、そのことを同一の試験パターンについて順次電子ビーム照射位置をずらし、2次電子の量に応じた濃淡画像を表示することが行われている。この場合の表示像は、例えば図7Aに示すように、ICの配線パターン像1～4が現れるが、高レベル電位が与えられている配線からの2次電子は少なく、表示画像においてパターン像1、2のように黒く表示される。一方、低レベル電位が与えられている配線からの2次電子は多く、表示画像においてパターン像3、4のように白く表示され、配線以外の部分15はその発生2次電子が高レベル部分及び低レベル部分における各2次電子の中間であって灰色に表示される。図6Aの画像をストロガ像と云う。

【0003】 この表示画像に対応する印加試験パターンが知られており、つまり、各配線の正常時の電位が知られているから、この表示画像を見て、そのICが正しく動作しているか、どの部分が異常であるか等の判断をすることができる。又、試験信号の設定したタイミング点から設定したタイミング点の間、電子ビームを位置水平走査させ、前記両タイミング点ごとに水平走査線を順次ずらして垂直走査し、例えば図7Aに示すように横軸が水平走査線の位置及び試験信号の時間軸を示す画像を形成することが行われている。図7Aにおいて配線パターン像は対応配線に図7Bに示す試験信号1aが印加され、そのタイミング点T₀からT₁までにおけるその配線の電位の経時変化を配線パターン像1は示し、従ってT₀から低レベルの部分ΔT₁は配線パターン像1に最初の白部分L₁として表示され、次の高レベル部分ΔT₂は配線パターン像1の次の部分L₂に黒部分として表示され、次の低レベル部分は配線パターン像1における次の白部分L₃として表示される。配線パターン像2及び3は試験信号2a及び3aがそれぞれ対応配線に印加され、そのタイミング点T₀乃至T₁の間に対応する像である。このように試験信号の時間変化も表示するよう

3

にした像はLSM像と呼ばれている。これは1画面で時間的変化の状態を知ることができる。

【0004】

【発明が解決しようとする課題】図6Aに示した像を得る場合にそのSN比を高くするため、同一画像をくり返し取得すると、ICの表面の絶縁保護膜に電荷が溜まり6B、6Cに示すように高レベルの配線パターン像と低レベルの配線パターン像との区別ができなくなり、ついには同一の灰色の表示となってしまう。従って高いSN比のものを得ることができなかった。

【0005】又、図6Aに示したように、試験信号の設定パターンにおけるデータを取りこむ場合は、その試験パターンの印加に基く変化の経時状態を知ることができない。しかし、LSM像ではこれを知ることができるが、図7について先に述べたようにLSM像を得る場合も同一条件でくり返し取得すると像が不明瞭になり、SN比を向上させることはできなかった。

【0006】更に、動作を保持する順次回路と、動作を保持しない論理回路とが複数従続的に設けられているICにおいては、その不良の発生段(場所)と試験信号における不良発生タイミングを知るには多くの画像を取得する必要があった。

【0007】

【課題を解決するための手段】この発明によれば、試験信号発生器から受信したトリガ信号は遅延手段により遅延されて、荷電粒子線パルスが発生させるが、その遅延量は、荷電粒子線によるICに対する水平又は垂直走査位置と対応して設定される。又、試験信号発生器からICの動作条件を変更したことを示す条件信号を受信することに、画像データの蓄積領域が切り替えられる。この動作条件の変更は、所定量の画像データ、例えば1画面分のデータを取得することに行われる。

【0008】画像データの表示は、現に取得中のものを表示する場合、2つの蓄積領域内の両画像データの差を表示する場合、この差の画像データとICのパターン形状情報とを重畳して表示する場合等がある。遅延手段による遅延は水平又は垂直走査の単位移動ごとに設定遅延量に対して所定遅延量ずつ加算させる。或いは、ICの走査をランダムに行わせ、そのランダム装置に水平又は垂直位置において、予め記憶された遅延データを読み出して、その遅延データを遅延回路に設定することにより行われる。

【0009】

【実施例】図1にこの発明の実施例を示す。荷電粒子線試験装置11として電子ビーム試験装置が用いられた場合で、この試験装置11に試験信号発生器12が接続される。電子ビーム試験装置11において、真空チャンパー13内で電子ビーム14がパルス状に発生され、チャンパー13内のIC15に照射される。その照射により発生した2次電子が2次電子検出器16で検出され、画

4

像データとして切替手段17により、画像メモリ18、19のいずれかに記憶される。

【0010】試験信号発生器内の試験パターン発生部21から発生された試験パターン信号や電源信号等が試験信号としてIC15へ供給され、IC15がこれに基いて動作する。その試験パターン信号のくり返しと同期して、つまり各試験パターン信号の始めにトリガ信号発生部22からトリガ信号が電子ビーム試験装置11内の遅延手段23へ供給される。更に、動作電源電圧等のIC15に対する動作条件を変更すると、そのことを示す条件信号が条件信号発生部24から電子ビーム試験装置11の制御部25に供給される。図に示していないが、制御部25に対して電子ビーム試験装置11の各種試験条件を設定することができ、その設定に応じて制御部25は各部を制御する。X走査手段26、Y走査手段27も制御部25により制御され、これら走査手段26、27により電子ビーム14が制御されて、IC15の設定された部分を水平・垂直走査する。

【0011】例えば図2Aに示す試験信号が発生され、その繰返し時点にトリガ信号が図2Bに示すように発生され、制御部25にトリガ信号に対し、図2Cに示すようにタイミング点 T_0 から T_1 までのデータの取込みとして設定され、また1水平走査線につき取込むデータ数がN個と設定されると、 $(T_1 - T_0) / (N - 1)$ の単位時間 Δt が求められ、遅延手段23の遅延量が $t_1 = T_0$ と初期設定される。最初のトリガ信号に遅延手段23で $t_1 = T_0$ だけ遅延されてパルス発生器29へ入力され、これより発生したパルスにより電子ビーム14のパルスが発射され、IC15の2次電子が検出される。以下トリガ信号ごとに図2Dに示すように $t_1 = T_0$ に対し、順次 Δt だけ多く遅延された電子ビームパルスが発射され、画像データの取込みが行われる。またこの1画像データの取込みごとに電子ビーム14は1画素分水平方向に移動される。つまりX走査手段26により電子ビーム14が1画素分水平方向に移動されることに、遅延手段23における設定遅延量が Δt だけ加算される。

【0012】このようにして1水平走査でタイミング $T_0 \sim T_1$ における画像データが取込まれ、同様に各水平走査ごと画像データが取込まれ、1画面分の画像データの取込みが終了すると、取得完了信号が試験信号発生器12へ送出される。この取得信号を受信すると試験信号発生器12はIC動作条件を変更し、例えば電源電圧を5Vから4Vに変更して条件信号を発生し、再び同様に試験信号、トリガ信号を発生し、電子ビーム試験装置11は図2について述べたように、各トリガ信号ごとに順次タイミングがずれた電子ビームパルスを発射して、画像データの取込みを行う。

【0013】以下同様に1画面分の画像データの取得ごとに取得完了信号を発生し、取得完了信号の受信ごとに

動作条件を交互に変更し、条件信号、試験信号、トリガ信号を発生することを繰返す。また条件信号の受信ごとに、画像データの取込みを画像メモリ18と19とに交互に切替える。IC15の動作電源電圧が5Vの場合にタイミング点 $T_0 \sim T_1$ 間における配線1', 2', 3'上の電位変化が図3Aの曲線1a, 2a, 3aと変化し、これが正常動作とする。これに対し、電源電圧が4Vに条件変更された場合にタイミング点 $T_0 \sim T_1$ 間における配線1', 2', 3'上の電位変化が図3Bの曲線1a, 2a, 3aに示すようになったとする。つまり配線1'は電位パターンの極性が反転し、配線2'は同一電位パターンとなり、配線3bはタイミング点 $T_2 \sim T_3$ だけ極性が反転した。

【0014】このような状態において繰返し画像データを取得し、その各画像データを表示部31に表示すると、図3Aの正常状態での取得画像は図3Cに示すようになる。即ち配線パターン像1は曲線1aの低レベルで白に表示され、高レベルで黒に表示される。配線パターン像2は、曲線2aが低レベル、高レベルにかかわりなく、灰色となっている、これは動作電源電圧が4Vに切替っても、同一電位曲線となるため、動作条件の切替えにかかわらず、配線2'における場所と時間とに対する電位状態は変化しないため、保護絶縁膜に対する充電が生じるためであり、つまり従来技術の問題点で指摘した場合と同一である。配線パターン像3は、そのタイミング点 $T_1 \sim T_3$ と対応する区間 L_{23} の低レベルでは白となり、その他の部分は、場所、時間について動作条件の切替えて変化が生じないため、灰色となる。

【0015】一方、図3Bの異常状態での取得画像は図3Dに示すようになる。即ち配線パターン像1は曲線1aの高レベルで黒、低レベルで白が表示され、配線パターン像2は図3Cの場合と同様に変化がないため灰色となり、配線パターン像3は動作切替えて変化が生じた曲線3aの区間 $T_2 \sim T_3$ の高レベルと対応する部分 L_{23} では黒、その他の部分は灰色となる。

【0016】このように図3C, Dから、動作状態を変更し、この例では電源電圧を4Vに下げると、配線1'では正常時と全く逆表示となり、異常となったことが理解され、しかも場所的、経時的にも常に正常時と異なったことが理解される。しかし配線2'では全く異常が生じないこともわかり、配線3'では配線3'上の部分 L_{23} で、タイミング $T_2 \sim T_3$ の区間だけ低レベルから高レベルに異常となったことが理解される。

【0017】更に図3Dに示した画像データから図3Cに示した画像データを引算し、その差の画像データを表示すると図4Aに示すようになる。つまり配線パターン像1は正常時の低レベルが高レベルになった部分 L_{04} 、 L_{56} は黒に、正常時の高レベルが低レベルになった部分 L_{45} 、 L_{61} は白に表示される。動作条件を変更しても異常とならなかった配線パターン像2は表示面上に全く現

われない。配線3'については低レベルから高レベルになった部分 L_{23} のみが黒となり、その他の部分は全く現われない。この図4Aの表示は異常となったものだけが図3C, Dの表示よりも、より明確に現われる。図3C, Dは異常の表示状態は図4Aの表示に対し、明確さが少し劣るが各配線パターン像も現われるため、不良個所の場所、時間的位置がよくわかる。

【0018】配線1'の電位が動作電源電圧5Vで図4Bの曲線1aの場合に、動作電源電圧を4Vに下げると、図4Bの曲線1a'のように、低レベルのままだった場合は、前記差画像データ像は図4C中の像 L_{23} のように高レベルが低レベルになった部分 T_{23} が白に表示される。更に曲線1a''のように曲線1a中の高レベル部分の前半 T_{24} が電源電圧の低下により低レベルになった場合は、差画像は部分 T_{24} のみが白の像 L_{24} として現われる。更に曲線1a'''のように曲線1aの高レベル部分の後半 T_{43} が低レベルになると、差画像は部分 T_{43} のみが白の像 L_{43} となって現われる。このようにこの発明では、配線電位の経時変化も知ることができる。なお曲線1a'', 1a'''の各場合はストロボ像ではそれぞれ黒、白表示となる。

【0019】IC15を動作させない状態で、その表面を電子ビーム走査して2次電子を検出し、あるいは試験信号を印加するが一定の状態のまま、繰返し電子ビーム走査して2次電子を検出してストロボ像を得るなどにより、IC15の表面の形状情報(画像データ)を取得し、つまり例えば図3Cの表示と対応するIC部分については、図4Dに示すように配線1', 2', 3'の配線パターン像1, 2, 3をそれぞれ2本線で表示することができるようにし、この形状情報をメモリ32に記憶しておき、この形状情報と差画像データ(図4Aと対応)とを重畳して表示することにより、注目すべき部分を明確に表示し、かつそのIC上の場所も読取り易いようにすることもできる。

【0020】上述では電子ビームの水平方向の移動と共に電子ビームの照射タイミングを Δt ずつ増加させたが、つまり表示面上の水平方向が時間軸となるように画像データを取得したが、垂直方向が時間軸となるように画像データを取得してもよい。この場合は、電子ビームの同一水平走査線上では、トリガ信号に対する電子ビーム照射タイミングを一定値 t_1 とし、次の水平走査線上では電子ビーム照射タイミングを Δt だけ遅らせ、トリガ信号に対し、 $t_1 + \Delta t$ のタイミングで電子ビームの照射を行う。なお1水平走査において、同一点を照射しないように、1画像データを取得するごとに、 Δt だけ水平走査の開始を早くするとよい。

【0021】1水平走査中に、電子ビームの照射タイミングを Δt ずつ増加させる場合に、垂直走査をランダムに行わせてもよい、つまり水平走査線の番号をランダムに並べ、その並べられた水平走査線番号を、各1水平走

7

査ごとに順次選択する。また前述したように時間軸が垂直方向となるように画像データを取得する場合において、各水平走査を、その線上の各画素位置番号をランダムに並べ、その並べた順に選択した画素位置に電子ビームを照射するようにしてもよい。これらのように水平又は垂直走査をランダムに行うことにより、接近した個所を連続して電子ビーム照射することが避けられ、保護絶縁膜のチャージの影響を少なくすることができる。この手法は特に位置分解能を高くする場合に有効である。

【0022】同様に水平・垂直走査をランダムにさせてもよい。例えば図5に示すように、水平走査上の各点に電子ビームを偏向させるに必要なデータが水平偏向レジスタ34に記憶され、垂直走査上の各点に電子ビームを偏向させるに必要なデータが垂直偏向レジスタ35に記憶され、1水平走査線上の各画素点に対する電子ビーム照射タイミング（トリガ信号に対する遅れ量）を示すデータが遅延レジスタ36に記憶されている。全走査面の各点の位置を示す番号がランダム発生器36から発生され、その下位ビットをアドレスとして水平偏向レジスタ34と遅延レジスタ36が上位ビットをアドレスとして垂直偏向レジスタ35がそれぞれ読出され、水平偏向レジスタ34から読出されたデータがDA変換器38でアナログ信号に変換されて水平方向偏向器へ供給され、垂直偏向レジスタ35から読出されたデータがDA変換器39でアナログ信号に変換されて垂直偏向器へ供給され、遅延レジスタ36から読出されたデータがトリガ信号を遅延する遅延回路41に設定され、その遅延回路41の出力がパルス発生器29へ供給される。

【0023】上述において、二つの動作条件での画像データを交互に取得するが、同一動作条件のものについて、それぞれ加算平均してSN比を向上させることもで

8

きる。1画面分の画像データを取込むに必要な時間は設定条件にもよるが、その最大の時間を見込み、試験信号発生器12側で、自動的に動作条件を変更し、電子ビーム試験装置11側では取得完了信号を発生しなくてもよい。1画面分のデータの取得ごとに動作条件をかえたが、半画面分のデータの取得ごとなど所定の画面分のデータの取得ごとに動作条件をかえてもよい。

【0024】

【発明の効果】以上述べたようにこの発明によれば電源電圧、試験パターンクロック周波数などの動作条件を、所定画面分のLSM像データを取得ごとに交互に切替えているため、注目している所を絶縁保護膜に影響されずに明確に得ることができる。

【図面の簡単な説明】

【図1】この発明の実施例を示すブロック図。

【図2】図1の動作における試験信号と、トリガ信号と、画像データ取得期間と、電子ビームパルス照射タイミングとの関係例を示す図。

【図3】A及びBは配線上の信号例を示す図、C及びDはそれぞれ対応取得画像データの表示例を示す図である。

【図4】Aは差画像データの表示例を示す図、Bは配線上の正常信号とその各種異常信号とを示す図、CはBにおける各異常信号と対応した表示画像を示す図、DはI Cの表面形状情報の表示画面の例を示す図である。

【図5】ランダム走査信号発生手段及び対応した遅延手段23の例を示すブロック図。

【図6】従来装置における問題点を説明するためのストロブ画像表示例を示す図。

【図7】AはLSM像表示の例を示す図、Bはその対応配線上の信号を示す図である。

【図2】

図 2

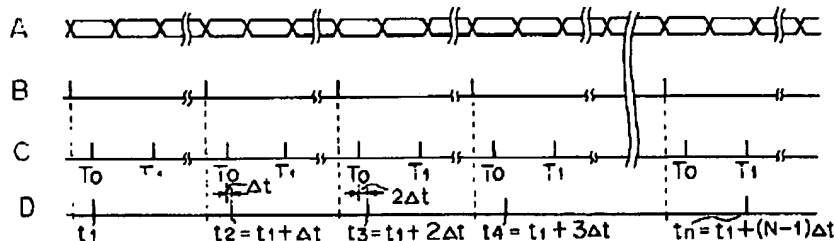
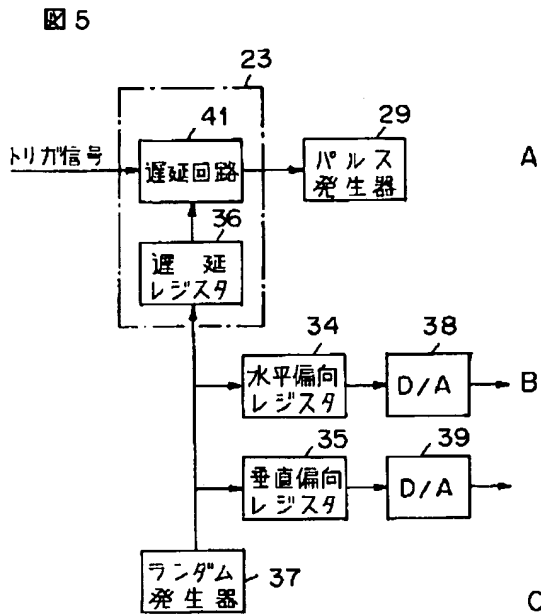


図 1

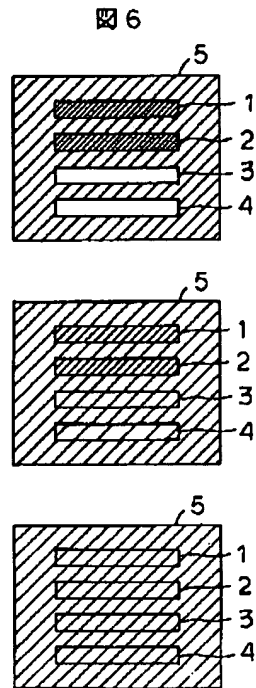
【図4】

Figure 1 consists of four schematic diagrams labeled A, B, C, and D. Diagram A is a top view of a rectangular structure with a central region labeled L23. The structure is divided into four quadrants by a horizontal and a vertical dashed line. The quadrants are labeled L04 (top-left), L45 (top-right), L56 (bottom-left), and L61 (bottom-right). The top and bottom edges are labeled T0 and T1. Diagram B is a cross-sectional view showing four layers labeled 1a, 1a', 1a'', and 1a''' from top to bottom. The top and bottom edges are labeled T0 and T1. Three time intervals are indicated: T23 between layers 1a and 1a', T24 between layers 1a'' and 1a''', and T43 between layers 1a' and 1a''. Diagram C is a cross-sectional view showing three layers labeled L23, L24, and L43 from top to bottom. The top and bottom edges are labeled T0 and T1. Diagram D is a cross-sectional view showing three layers labeled 1, 2, and 3 from top to bottom. The top and bottom edges are labeled T0 and T1.

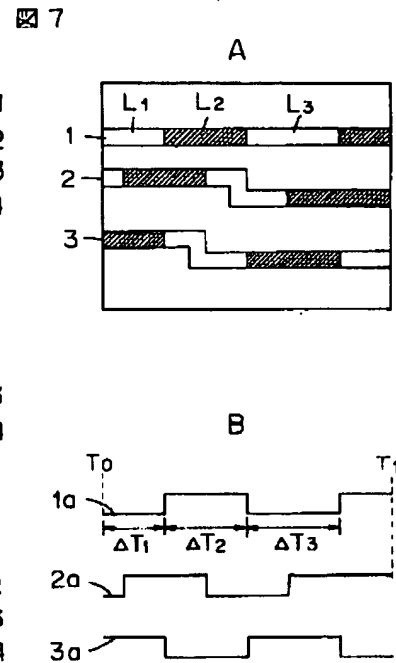
【図5】



【図6】



【図7】



フロントページの続き

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